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10/590,613	08/24/2006	Andrey Efimov	42P23458	8961

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AHMED, ENAM	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,613	EFIMOV ET AL.	
	Examiner	Art Unit	
	ENAM AHMED	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/27/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non – Final

35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 16 and 21 are rejected under 35 U.S.C. 102(b) as being unpatentable over Vasic et al. (U.S. Patent No. 6,691,263).

With respect to claim 1, the Vasic et al. reference teaches a plurality of processing elements, that process data based on content of the data stored in a plurality of associated memory, to iteratively decode a received codeword using a bit reliability such that for each iteration the bit reliability is updated based on a comparison using a threshold comprising a plurality of threshold values that are updated during the iterative decoding (column 7, lines 26-43).

With respect to claim 16, the Vasic et al. reference teaches wherein the processing elements continue to iteratively decode the low-density parity check codeword for log2 n number of iterations, where n is a code length of the codeword (column 7, lines 26-43).

With respect to claim 21, the Vasic et al. reference teaches comprising a transmitter (see fig. 1, 101) ,a network interface to receive one or more codewords over a communication medium (see fig. 1, 103),a receiver comprising a demodulator to generate soft decisions for the one or more codewords based on one or more characteristics of the communication medium and a decoder comprising a plurality of processing elements, processing data based on content of the data stored in a plurality of associated memory, to iteratively decode a first codeword of the one or more codewords using a bit reliability such that for each iteration the bit reliability is updated based on a comparison using a threshold comprising a plurality of threshold values that are updated during the iterative decoding (column 7, lines 26-43).

35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 10-15 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasic et al. (U.S. Patent No. 6,691,263) in view of Hocevar (U.S. Patent No. 7,139,959).

With respect to claim 2, all of the limitations of claim 1 have been addressed. The Vasic et al. reference does not teach wherein the plurality of processing elements comprise input processing elements, row control elements, column control elements, and associative processing elements arranged in one or more rows and columns based on a presence of a first logic level present in each row and column of a low-density parity check matrix. The Hocevar reference teaches wherein the plurality of processing elements comprise input processing elements, row control elements, column control elements, and associative processing elements arranged in one or more rows and columns based on a presence of a first logic level present in each row and column of a low-density parity check matrix (column 19, lines 9-24). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Vasic et al. with Hocevar to incorporate wherein the plurality of processing elements comprise input processing elements, row control elements, column control elements, and associative processing elements arranged in one or more rows and columns based on a presence of a first logic level present in each row and column of a low-density parity check matrix into the claimed invention. The motivation for wherein the plurality of processing elements comprise input processing elements, row control elements, column control elements, and associative processing elements arranged in one or more rows and columns based on a presence of a first logic level present in each row and column of a low-density parity check matrix is for improved system performance.

With respect to claim 3, the Vasic et al. reference teaches an input processing element that determines an initial bit reliability and an initial hard decision value for bit positions of a

codeword based on soft decision values, wherein the codeword is generated based on the low-density parity check parity matrix and the soft decision values are generated based on a likelihood that a bit represents a first value (column 7, lines 26-43).

With respect to claim 4, the Vasic et al. reference teaches wherein the input processing element generates the initial bit reliability as equaling an absolute value of a value corresponding to the bit positions, and the initial hard decision value as equaling a second value if the soft decision value is positive and a third value otherwise (column 7, lines 26-43).

With respect to claim 10, the Vasic et al. reference teaches wherein a first column of the columns comprise a first input processing element, a first column control element, and a second set of the associative processing elements, which, collectively, determine a first bit of an updated hard decision vector (column 8, lines 24-43).

With respect to claim 11, the Vasic et al. reference teaches wherein the first input processing element, the first column control element, and the second set of the associative processing elements, collectively, determine a first bit of an updated hard decision vector based on a first comparison reliability value and a first threshold value of the plurality of threshold values (column 8, lines 24-43).

With respect to claim 12, the Vasic et al. reference teaches wherein the first input processing element, the first column control element, and the second set of the associative

processing elements, collectively, determine the first comparison reliability value based on a first check sum determined based on the hard decision values and a first minimum value representing a minimum value of the bit reliability stored in a first set of associative processing elements of a first row (column 8, lines 24-43).

With respect to claim 13, the Vasic et al. reference teaches wherein the processing elements determine the plurality of threshold values based on a first characteristic of a communication channel over which the low-density parity check codeword is received (column 7, lines 26-43).

With respect to claim 14, the Vasic et al. reference teaches wherein the processing elements continue to iteratively decode the low-density parity check codeword until a desired data stream is generated (column 7, lines 26-43).

With respect to claim 15, the Vasic et al. reference teaches wherein the processing elements continue to iteratively decode the low-density parity check codeword for log2 n number of iterations, where n is a code length of the codeword (column 7, lines 26-43).

With respect to claim 22, the Vasic et al. reference teaches wherein the receiver receives the one or more codewords at a rate of at least 10 giga bits per second in accordance with 10GBase-T standard (column 7, 29-31).

With respect to claim 23, the Vasic et al. reference teaches generating the one or more codewords by encoding a bit stream based on a low-density parity check codes and sending the one or more codewords over the communication medium (column 7, lines 31-36), and the network interface to transmit the one or more codewords at a rate of at least 10 giga bits over the communication medium (column 7, lines 31-36).

With respect to claim 24, the Vasic et al. reference teaches a network interface card (see fig. 1, 103).

With respect to claim 25, the Vasic et al. reference teaches at least one of a computer, a switch, a router, a handheld, a cell phone, or a server (see fig. 1, 103).

Claims 5-6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasic et al. (U.S. Patent No. 6,691,263), Hocevar (U.S. Patent No. 7,139,959) in view of Lee (U.S. Patent No. 6,421,804).

With respect to claim 5, all of the limitations of claim 2 have been addressed. The Vasic et al. reference does not teach wherein a first row of the rows comprises a first set of associative processing elements and a first row control element, which, collectively, determine a first minimum value and a second minimum value of bit reliability values stored in the first set of associative processing elements during a first iteration. The Lee reference teaches wherein a first row of the rows comprises a first set of associative processing elements and a first row control

element, which, collectively, determine a first minimum value and a second minimum value of bit reliability values stored in the first set of associative processing elements during a first iteration (column 4, lines 33-54). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Vasic et al. with Lee to incorporate wherein a first row of the rows comprises a first set of associative processing elements and a first row control element, which, collectively, determine a first minimum value and a second minimum value of bit reliability values stored in the first set of associative processing elements during a first iteration into the claimed invention. The motivation for wherein a first row of the rows comprises a first set of associative processing elements and a first row control element, which, collectively, determine a first minimum value and a second minimum value of bit reliability values stored in the first set of associative processing elements during a first iteration is for improved reliability.

With respect to claims 6 and 17, all of the limitations of claims 5 and 16 have been addressed. The Vasic et al. reference does not teach wherein the first row control element stores the first minimum value in the first set of associative processing element comprising a value other than the first minimum value, and stores the second minimum value in the first set of associative processing elements that stored the first minimum value before the first iteration. The Lee reference teaches wherein the first row control element stores the first minimum value in the first set of associative processing element comprising a value other than the first minimum value, and stores the second minimum value in the first set of associative processing elements that stored the first minimum value before the first iteration (column 4, lines 47-54). Thus, it would

have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Vasic et al. with Lee to incorporate wherein the first row control element stores the first minimum value in the first set of associative processing element comprising a value other than the first minimum value, and stores the second minimum value in the first set of associative processing elements that stored the first minimum value before the first iteration into the claimed invention. The motivation for wherein the first row control element stores the first minimum value in the first set of associative processing element comprising a value other than the first minimum value, and stores the second minimum value in the first set of associative processing elements that stored the first minimum value before the first iteration is for improved reliability.

Claims 7-9, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasic et al. (U.S. Patent No. 6,691,263), Hocevar (U.S. Patent No. 7,139,959), Lee (U.S. Patent No. 6,421,804) in view of Yu et al. (U.S. Patent No. 7,137,060).

With respect to claims 7 and 18, all of the limitations of claims 5 and 16 have been addressed. The Vasic et al. reference does not teach wherein the first row control element generates one or more control values comprising a first comparand and a mask to determine the presence of the first minimum value in the first set of associative processing element, a second comparand and a mask to determine the presence of the second minimum value in the first set of associative processing element, receives one or more decision values indicating presence of one or more of the first minimum value and the second minimum value, and determines the first

minimum value and the second minimum value based on the one or more decision values. The Yu et al. reference teaches wherein the first row control element generates one or more control values comprising a first comparand and a mask to determine the presence of the first minimum value in the first set of associative processing element, a second comparand and a mask to determine the presence of the second minimum value in the first set of associative processing element (column 11, lines 28-34), receives one or more decision values indicating presence of one or more of the first minimum value and the second minimum value (column 11, lines 35-48), and determines the first minimum value and the second minimum value based on the one or more decision values (column 11, lines 38-44). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Vasic et al. with Yu et al. to incorporate wherein the first row control element generates one or more control values comprising a first comparand and a mask to determine the presence of the first minimum value in the first set of associative processing element, a second comparand and a mask to determine the presence of the second minimum value in the first set of associative processing element, receives one or more decision values indicating presence of one or more of the first minimum value and the second minimum value, and determines the first minimum value and the second minimum value based on the one or more decision values into the claimed invention. The motivation for wherein the first row control element generates one or more control values comprising a first comparand and a mask to determine the presence of the first minimum value in the first set of associative processing element, a second comparand and a mask to determine the presence of the second minimum value in the first set of associative processing element, receives one or more decision values indicating presence of one or more of

the first minimum value and the second minimum value, and determines the first minimum value and the second minimum value based on the one or more decision values is for improved reliability.

With respect to claims 8 and 20, the Vasic et al. reference teaches wherein the first set of associative processing elements receive the one or more control values (column 4, lines 3-5), and generate the one or more decision values comprising a first value indicating a presence of the first minimum value in at least one of the first associative processing elements, a second value indicating a presence of the second minimum value in at least one of the first associative processing elements, and a third value indicating a presence of the first minimum value in at least two of the first associative processing elements (column 4, lines 6-17).

With respect to claim 9, the Vasic et al. reference teaches a logic to receive the one or more control values and generate update values, wherein the update values represent a result of comparison of masked on bits of the first comparand and the bit reliability value stored in the first element (column 4, lines 6-17), and a set of logic gates to generate the one or more decision values based on the update values and send the decision values to a second element (column 4, lines 10-17).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman, can be reached on 571-272-3644.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

12/16/09

/MUJTABA K CHAUDRY/

Primary Examiner, Art Unit 2112